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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/598,926	06/21/2000	Martin Vorbach	2885/31	6326

26646 7590 01/21/2003

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EXAMINER
MOORE, WILLIAM P

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 01/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/598,926	Applicant(s) VORBACH ET AL.	
	Examiner William P Moore	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-35* is/are pending in the application.

4a) Of the above claim(s) *1-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *18-22,24,25,27 and 29-35* is/are rejected.

7)☐ Claim(s) *23, 26, 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *22 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4,6,8,10* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Detailed Office Action

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on application DE-197-57-200-6 filed in Germany on December 22, 1997. It is noted, however, that the applicant has not filed a certified translation of the application as required by 35 U.S.C. 119(b).

Claim Rejections - 35 USC § 102

Statement of Statutory Basis

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 18, 19, 20, 21, 22, 24, 25, 27, 29, and 35

3. Claim 18, 19, 20, 21, 22, 24, 25, 27, and 35 are rejected under 35 U.S.C 102(b) as being clearly anticipated by Hefner (US Patent 4,566,102).

As per claim 18, 19, 20, 21, 22, 24, 25, 27, and 35, Hefner substantially teaches the claimed integrated circuit arrangement, comprising :

at least one module including one of an individual module and a plurality of ordered modules (See Figure 2, modules titled "Byte Array 0" to "Byte Array 7".) ,

each module of the at least one module having at least one input and at least one output (See Figure 2, input and outputs of modules titled "Byte Array 0" to "Byte Array 7".),

the at least one module forming at least one cell (A module is a type of cell. See applicant' definition for cell on page 25, ll. 17-18.),

the at least one cell including at least one of a bus system, an arithmetic and logic unit and a configurable logic cell (See Col 1, ll. 65 to Col 2, ll. 1 where Hefner discloses that invention is applicable to vector element processors in place of array elements shown in figure 2. It is old and well known in the art that a processor is a type of ALU and as such includes a bus for inputting and output data and is configurable to perform an ALU operation.);

a supplementary module assigned to the at least one module and being of a same kind as the at least one module (See Figure 2, module labeled "Spare array");

a first switching element coupled to the at least one input of a particular module and being upstream from the at least one input of the particular module (See Figure 2 where first switching elements shown as thick arrow 21 and adjacent arrows. These switching elements are respectively attached upstream from module 11 and adjacent modules. The state of the switching elements is shown as black for 'on' and white for 'off'. The switching elements are controlled by selects A/B Ctl 23, and CIPT 25. The operation of said switching element is described in col. 3, ll. 17-35.);

the first switching element switching an input signal to at least one of the particular module and a module following the particular module (Col. 3, lines 19-20. Also, see Figure 2 where input byte 0 and adjacent inputs, byte 1 to byte 7, are individually switched between two adjacent modules.);

a second switching element coupled to the at lest one output of the particular module and being downstream from the at least one output of the particular module (See Figure 2 where switching of output byte 0 and adjacent outputs, byte 1 to 7, are coupled downstream from two particular modules. For the case of output byte 0, the output is coupled downstream

to byte array 0 and byte array 1. The operation of this second switching element is described in col. 3, ll. 17-35);

wherein, if an error occurs in a module, then at least one of a defective module and a defective function cell is replaced by a module following the at least one of the defective module and the defective function cell by switching the first switching element and by switching the second switching element, a last module being replaced by the supplementary module. (See claim 4 that substantially describes this operation. Also, see specification in reference to figure 2 and 3. The first switching elements 21 are shown by thick arrows at the top of the figures. The second switching elements 24 and 22 are shown by thick arrows at the bottom of the figures. In figures 2 and 3, the state of the switch is shown by the color of the arrow. A thick black arrow meaning that the switch is on and a thick white arrow means the switch is off. Figure 2, shows the case where there is no error and figure 3 show the case where there is an error in the module that formally held byte array 5. As is apparent from figure 3, the defective module has been replace by the adjacent module and the former spare/supplementary module now holds byte array 7.)

As per claim 19, Hefner further teaches that the error is detected via self-testing. (col. 2, lines 56-60; col. 3, lines 60-63)

As per claim 20, Hefner further teaches a control that controls the first switching element and the second switching element (Controls are shown in Figure 2 as A/B Ctl 23 and CIPT 25. The operation of these control signals are described in Col 3. lines 19-35), with at least one of:

(A) the control switching all of the switching elements in the same way (See Figure 4, top and bottom row of truth table for control signal A/B Ctl. Since B0 to BS are the same value then all switching elements are the same way)

(B) all of the switching elements forming a first group of switching elements and a second group of switching elements. (See Figure 4, tabled "A/B Ctl. Outputs". This table shows all possible switching patterns with two distinct switching groups where each row represents one possible switch configuration. Its is apparent from inspection of each row that the control bits on the left hand side with the value of '1' form one group that selects the 'B' data path and the bits on the right hand side with the value of '0' selects the A data path. This grouping of elements is further apparent by considering the manner in which the device operates to correct defects by "shifting over one unit in the direction of the spare unit the content of the failed unit and the spare unit", Col 2, lines 1-5. Thus, all units preceding the defective unit form one group by being configured normally and all units after the defective unit form a second group by being configured to shift by one unit.)

As per claim 21, Hefner further teaches that the control is adapted to decode a binary value so as to yield at least one of the first group and the second group. (See col. 3, line 58 to col. 3, line 3, col. 4., lines 17-23. Also, see figure 4 where the table "config. ctl. reg." defines all possible encoded binary values that are decoded to produces control signals CIPT and CTL for switching a first and second groups as per claim 20.)

As per claim 22, Hefner further teaches that the control is adapted to encode a binary value, the binary value defining at least one of a switching element group and a switching element circuit. (See col.. 3, line 58 to col. 3, line 3, where 4-bit binary value is encoded into latches that controls signals CIPT and A/B CTL, Col. 4, lines 17-23, the control signals for switching a first and second groups as per claim 20.)

As per claim 24, Hefner further teaches that the binary value is provided via a look-up-table arrangement. (See Figure 4 where the binary decoded value, shown as CIPT and A/B CTL, is provided by a lookup table where Config. Ctl Reg. is the lookup

index. This operation is described in col. 3, line 58 to col. 3, line 3, and col. 4., lines 17-23.)

As per claim 25, Hefner further teaches a memory that stores a binary value, the binary value indicating at least one of the defective module and all defective modules. (col. 3, line 58 to col. 3, line 3 that describes a 4-bit latch which is a type of memory defined by bits C0, C1, C2, and SP. This latch is for hold an encoded binary value that indicates the defective module, col. 3 line 63 to col. 3, line 3)

As per claim 27, Hefner further teaches a method for testing an integrated circuit having cells, comprising the steps of:

testing a cell function of the integrated circuit by executing, with the cells a test program including calculating test vectors (See col. 2, lines 56-60, since output of array cells 13 are used to generate parity for checking the functionality of the array, the outputs of the array cell is a test vector. Col 1., lines 65 to col. 2., line 1 discloses that array cell can be a vector processor element, thus Hefner has anticipated the use of a program a test program because a vector processor element is a type of ALU.)

performing, with at least one of the cells, a comparison between a test result and a setpoint result(col. 1, lines 65 to col. 2, line 1, teaches that a maintenance processor, i.e. a type of cell, performs parity checking on the outputs of the array cells, thus this system inherently contains a comparison between the actual parity calculated from the array output cells and the expected parity, i.e. set point result, in order to diagnosis a failed array cell.);

indicating an error if the comparison indicates a deviation between the setpoint result and the test result so that, in response to the error, a module having the cell found to be defective is replaced. (col. 2, lines 1-12, teaches replacement of failed array cells. Col 2, lines 55-60, teaches failure diagnostics isolation of array cells, i.e. indicating an error)

As per claim 35, Hefner further teaches the method according to claim 27, further comprising the steps of:

assigning at least one additional supplementary module to a number of ordered modules forming the cells (See Figure 2, modules titled "Byte Array 0" to "Byte Array 7" represent the ordered modules. The module title "Spare Array" represents the supplementary module),

the at least one additional supplementary module and the ordered modules being of the same kind, (Col 2, lines 1-5, since supplementary module is a spare for ordered modules it but be the same size),

each module having at least one input and at least one output (See Figure 2, input and outputs of modules titled "Byte Array 0" to "Byte Array 7".),

coupling a first switching element to the at least one input of a particular module and being disposed upstream from the at least one input of the particular module (See Figure 2 where first switching elements shown as thick arrow 21 and adjacent arrows. These switching elements are respectively attached upstream from module 11 and adjacent modules. The state of the switching elements is shown as black for 'on' and white for 'off'. The switching elements are controlled by selects A/B Ctl 23, and CIPT 25. The operation of the switch is described in col. 3, ll. 17-35.),

the first switching element being adapted to switch an input signal to one of the particular module and a module following the particular module (Col. 3, lines 19-20. Also, see Figure 2 where input byte 0 and adjacent inputs, byte 1 to byte 7, are individually switched between two adjacent modules.);

coupling a second switching element to the at least one output of the particular module and being disposed downstream from the at least one output of the

particular module and being adapted to receive an output from one of the particular module and the module following the particular module (See Figure 2 where switching of output byte 0 and adjacent outputs, byte 1 to 7, are coupled downstream from two particular modules. For the case of output byte 0, the output is coupled downstream to byte array 0 and byte array 1. The operation of this second switching element is described in col. 3, ll. 17-35);

wherein, if an error is detected in a module, then replacing a defective module by a module following the defective module by switching the first switching element and the second switching element, a last module in the ordered modules being-replaced by the-supplementary module (See claim 4 that substantially describes this operation. Also, see specification in reference to figure 2 and 3. The first switching elements 21 are shown by thick arrows at the top of the figures. The second switching elements 24 and 22 are shown by thick arrows at the bottom of the figures. In figures 2 and 3, the state of the switch is shown by the color of the arrow. A thick black arrow meaning that the switch is on and a thick white arrow means the switch is off. Figure 2, shows the case where there is no error and figure 3 show the case where there is an error in the module that formally held byte array 5. As is apparent from figure 3, the defective module has been replace by the adjacent module and the former spare/supplementary module now holds byte array 7.).

As per claim 35, Hefner further teaches the method according to claim 27, further comprising the steps of:

assigning at least one additional supplementary module to a number of ordered modules forming the cells (See Figure 2, modules titled "Byte Array 0" to "Byte Array 7" represent the ordered modules. The module title "Spare Array" represents the supplementary module),

the at least one additional supplementary module and the ordered modules being of the same kind, (Col 2, lines 1-5, since supplementary module is a spare for ordered modules it but be the same size),

each module having at least one input and at least one output (See Figure 2, input and outputs of modules titled "Byte Array 0" to "Byte Array 7".),

coupling a first switching element to the at least one input of a particular module and being disposed upstream from the at least one input of the particular module (See Figure 2 where first switching elements shown as thick arrow 21 and adjacent arrows. These switching elements are respectively attached upstream from module 11 and adjacent modules. The state of the switching elements is shown as black for 'on' and white for 'off'. The switching elements are controlled by selects A/B Ctl 23, and CIPT 25. The operation of the switch is described in col. 3, ll. 17-35.),

the first switching element being adapted to switch an input signal to one of the particular module and a module following the particular module (Col. 3, lines 19-20. Also, see Figure 2 where input byte 0 and adjacent inputs, byte 1 to byte 7, are individually switched between two adjacent modules.);

coupling a second switching element to the at least one output of the particular module and being disposed downstream from the at least one output of the particular module and being adapted to receive an output from one of the particular module and the module following the particular module (See Figure 2 where switching of output byte 0 and adjacent outputs, byte 1 to 7, are coupled downstream from two particular modules. For the case of output byte 0, the output is coupled downstream to byte array 0 and byte array 1. The operation of this second switching element is described in col. 3, ll. 17-35);

wherein, if an error is detected in a module, then replacing a defective module by a module following the defective module by switching the first switching element and the second switching element, a last module in the ordered modules being-replaced by the-supplementary module (See claim 4 that substantially describes this operation. Also, see specification in reference to figure 2 and 3. The first switching elements 21 are shown by thick arrows at the top of the figures. The second switching elements 24 and 22 are shown by thick arrows at the bottom of the figures. In figures 2 and 3, the state of the switch is shown by the color of the arrow. A thick black arrow meaning that the switch is on and a thick white arrow means the switch is off. Figure 2, shows the case where there is no error and figure 3 show the case where there is an error in the module that formally held byte array 5. As is apparent from figure 3, the defective module has been replace by the adjacent module and the former spare/supplementary module now holds byte array 7.).

As per claim 29, Hefner implicitly teaches wherein the step of testing the cell function includes the step of calling up test data from an integrated memory in the integrated circuit, the test data being used for executing the test program. (Since col. 1, lines 65 to col. 2, line 1, discloses that a vector processing element can be used for the array cells 11, and since a vector processing element is a type of ALU, the integrated circuit must inherently contain micro-code, i.e. program memory, for operating the vector processor element during all modes of operations.)

Claim Rejections - 35 USC 103

Statement of Statutory Basis

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a

person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 31, 33, and 34

5. Claim 31 and 33 are rejected under 35 USC 103(a) as being unpatentable over Hefner (US Patent 4,566,102) in view of Matsumoto (US Patent 5,657,330). Claim 34 is rejected under 35 USC 103(a) as being unpatentable over Hefner, Matsumoto and further in view of Takano (US Patent 5,530,873).

As per claim 31, 33 and 34, Hefner has taught all of the limitations described by claim 27. (See claim 27 rejection under USC 102(b))

Claim 31

As per claim 31, Hefner has not explicitly taught a method for testing the integrated circuit that is carried out as a self-test method of application programs running during at least one of await cycle and an IDLE cycle Matsumoto has taught this limitation in col. 1, lines 53 - 58. Hefner and Matsumoto are analogous art because they are from a similar problem solving area of integrated circuit test.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to apply testing mode, i.e. failure diagnostic isolation (Hefner, col. 2, lines 56-60) during IDLE or away cycles of vector processor elements (Hefner, col. 2, lines 65 to col. 2, line 1, array cells 11 maybe vector processor elements).

The motivation for doing so would have been to test vector processor elements in-circuit without using an external tester or modifying the circuit connections to other cells. (Matsumoto, col. 1, lines 14-24, and lines 32-49) Therefore, it would have been obvious to combine Hefner with Matsumoto to obtain the invention as specified in claim 31

Claim 33

As per claim 33, Hefner has not explicitly taught the steps of saving data from the arithmetic and logic units to a chip-internal memory before running a test algorithm; and loading data back into the arithmetic and logic units after running the test algorithm. Matsumoto has taught this limitation in figure 2, step S3 and S9. Further, it has been

previously established, as per claim 32, that it is obvious to apply testing mode, i.e. failure diagnostic isolation (Hefner, col. 2, lines 56-60) during IDLE or away cycles of vector processor elements (Hefner, col. 2, lines 65 to col. 2, line 1, array cells 11 maybe vector processor elements).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to further modify Hefner to program the vector processor elements (Hefner, col. 2, lines 65 to col. 2, line 1, array cells 11 maybe vector processor elements). to save and restore the context of internal registers when initializing test mode during IDLE or away cycles of vector processor elements.

The motivation for doing so would have been to test vector processor elements in-circuit without using an external tester or modifying connection to other cells. (Matsumoto, col. 1, lines 14-24, and lines 32-49) Therefore, it would have been obvious to combine Hefner with Matsumoto to obtain the invention as specified in claim 33.

Claim 34

As per claim 34, Hefner has not explicitly taught the method according to claim 33, further comprising the steps of:

shutting down registers in the arithmetic and logic units before running the test algorithm;

using test registers for the test algorithms;

connecting the registers in the arithmetic and logic units after running the test algorithm

Matsumoto has taught the use of context switching to execute a self-test procedure on a processor (Figure 2, shows context switching to and from self-test procedure) and executing the self-test procedure during the idle state of the processor (Col. 2 , lines 45-51).

Takano has taught the use of shadow registers for improved context switching (Col. 2, lines 14-26).

It has been previously established, as per claim 32, that it is obvious to apply testing mode, i.e. failure diagnostic isolation (Hefner, col. 2, lines 56-60) during IDLE

or away cycles of vector processor elements (Hefner, col. 2, lines 65 to col. 2, line 1, array cells 11 maybe vector processor elements).

Further, It has been previous established, as per claim 33, that it is obvious to program the vector processor elements (Hefner, col. 2, lines 65 to col. 2, line 1, array cells 11 maybe vector processor elements). to save and restore the context of internal registers when initializing test mode during IDLE or away cycles of vector processor elements.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to add a bank of shadow registers (Fig 3, shadow registers for every ordinary register) to the vector processor element for the purpose of fast context switching between applicant program and test program. So that when initializing the test program the normal processor registers are shut down and test program registers are used in their place (col. 2, lines. 21-22) Then, executing the test program and then reconnecting the normal processor registers (col. 2, lines 26-27).

The motivation for doing so would have been to increase the speed of context switching over conventional methods of saving and restoring registers from memory (col. 2, lines 14-17).

Claim 30

6. Claim 30 is rejected under 35 USC 103(a) as being unpatentable over Hefner (US Patent 4,566,102) in view of Bouvier et al. (US Patent 5,530,946).

As per claim 30, Hefner has not explicitly taught a method for testing the integrated circuit that is carried out at system start. Bouvier et al. taught that testing procedures can be invoked in subroutines of the initialization code for a processor system, i.e. at system startup. Hefner and Bouvier et al. are analogous art because they are from a similar problem solving area of integrated circuit test.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify Hefner such that the vector processor elements (Hefner, col. 2, lines 65 to col. 2, line 1, array cells 11 maybe vector processor elements) executes a self-testing procedure at system startup.

The motivation for doing so would have been to provide failure and fault recovery between two array cells in the integrated circuit (col. 1, lines 9-12).

Claim 32

7. Claim 32 is rejected under 35 USC 103(a) as being unpatentable over Hefner (US Patent 4,566,102) in view of Bouvier et al. (US Patent 5,530,946).

As per claim 32, Hefner has not explicitly taught a self-test method that is called up from an application program and integrated into an application program. Bouvier et al. (US Patent 5,530,946) has taught that a self-testing procedures can be invoked in subroutines of the initialization code for a processor system, i.e. at system startup. Hefner and Bouvier et al. are analogous art because they are from a similar problem solving area of integrated circuit test.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify Hefner such that the vector processor elements (Hefner, col. 2, lines 65 to col. 2, line 1, array cells 11 maybe vector processor elements) executes a self-testing procedure at system startup as part of the application program of the vector processor.

The motivation for doing so would have been to provide failure and fault recovery between two array cells in the integrated circuit (col. 1, lines 9-12).

Allowable Subject Matter

Claims 23, 26 and 28

8. Claim 23, 26, and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As per claim 23, the primary reason for allowance is because the closest reference Hefner (US Patent 4,566,102) does not teach the limitation that the binary value is generated by a counter.

As per claim 26, the primary reason for allowance is because the closest reference Hefner (US Patent 4,566,102) does not teach that the memory is independent of a system start.

As per claim 28, the primary reason for allowance is because the closest reference Hefner (US Patent 4,566,102) does not teach the step of testing the cell function includes the step of testing a cell array by at least one of exchanging and mirroring a test algorithm that includes a plurality of calculations at least once within the cell array.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Patrick Moore whose telephone number is (703)305-9727. The examiner can normally be reached on 8:30 - 5 PM If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703)305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 746-7240.

William Patrick Moore
January 6, 2003

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